What is claimed is:

1. A method for bootstrapping a processor from a volatile memory device connected to the processor, comprising the steps of:

bootstrapping a first processor from flash device;

asserting reset lines of the second processor;

loading boot code for the second processor from the flash device into the volatile memory device; and

de-asserting the reset lines of the second processor, wherein the processor performs the bootstrap procedure using the boot code stored in the volatile memory device.

2. The method according to claim 1, wherein the memory control signals of the second processor and hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device.

3. The method according to claim 1, wherein a complex programmable logic device generates the reset lines of the processor.

4. The method according to claim 3, wherein the reset lines are controlled by the first processor and handled by the complex programmable logic device.

5. The method according to claim 2, wherein a complex programmable logic device comprises logic units to correctly combine the memory control signals of the second processor and the hardware handshake signals of the volatile memory device.

6. The method according to claim 1, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device.

7. The method according to claim 6, wherein the first processor provides identity to each of the plurality of processors by posting information through volatile memory.

8. The method according to claim 1, wherein the volatile memory device is static random access memory.

9. The method according to claim 1, wherein the volatile memory device is dual port random access memory.

10. The method according to claim 8, wherein the volatile memory device is a synchronous static random access memory.

11. The method according to claim 8, wherein the volatile memory device is a synchronous dual port static random access memory.

12. The method according to claim 10, wherein the synchronous static random access memory has a discontinuous clock throughout the bootstrapping procedure.

13. A system for bootstrapping a processor from a volatile memory device, comprising:

a second processor with associated flash device;

a logic device for generating reset lines of the second processor and deasserting the reset lines based on control signals from the first processor;

the volatile memory device for storing boot code for the second microprocessor loaded from the flash device after the first processor has been bootstrapped; and

the processor connected to the volatile memory device, wherein when the reset lines of the second processor are de-asserted, the second processor bootstraps from the boot code stored in the volatile memory device.

14. The system according to claim 13, wherein the boot code of the processor and hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device.

15. The system according to claim 13, wherein the logic unit is a complex programmable logic device.

16. The system according to claim 15, wherein the logic unit is a field programmable gate array.

17. The system according to claim 15, wherein the complex programmable logic device comprises logic units to correctly combine the memory control signals of the processor and the hardware handshake signals of the volatile memory device.

18. The system according to claim 13, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device.

19. The system according to claim 18, wherein the master processor provides identity to each of the plurality of processors by posting information through volatile memory.

20. The system according to claim 13, wherein the volatile memory device is static random access memory.

21. The system according to claim 13, wherein the volatile memory device is dual port random access memory.

22. The system according to claim 19, wherein the volatile memory device is a synchronous static random access memory.

23. The system according to claim 22, wherein the pipeline static random access memory has a discontinuous clock through out the bootstrapping procedure.

24. The system according to claim 13, further comprising:
a flash device connected to the second processor having boot code for the processor, wherein the first processor determines whether to bootstrap the second processor using the boot code in the flash device connected to the second processor or the boot code in the volatile memory device based on a user selection.

25. The system according to claim 24, wherein the first processor sets a command register in the logic device to configure logic units for the selected bootstrap procedure.

26. A method for bootstrapping a processor from either a flash device or a volatile memory device, comprising the steps of:

bootstrapping a master processor;

determining whether a flash bootstrap procedure or a volatile memory device bootstrap procedure has been selected for the second microprocessor;

setting a command register in a logic device to configure logic units for the selected bootstrap procedure;

if the flash bootstrap procedure was selected:

performing bootstrap procedure from the flash device associated with the second processor;

if the volatile memory bootstrap procedure was selected:

asserting reset lines of the processor;

loading boot code for the second processor from a flash device associated with the first processor into the volatile memory device; and

de-asserting the reset lines of the processor, wherein the processor bootstraps from the boot code stored in the volatile memory device.

27. The method according to claim 26, wherein the memory control signals of the second processor and hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device.

28. The method according to claim 26, wherein a complex programmable logic device generates the reset lines of the second processor.

29. The method according to claim 28, wherein the reset lines are controlled by the master processor.

30. The method according to claim 26, wherein a complex programmable logic device comprises logic units to correctly combine memory control signals of the processor and the hardware handshake signals of the volatile memory device.

31. The method according to claim 26, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device.

32. The method according to claim 31, wherein the master processor provides identity to each of the plurality of processors by posting information through shared memory.

33. The method according to claim 26, wherein the volatile memory device is static random access memory.

34. The method according to claim 26, wherein the volatile memory device is dual port random access memory.

35. The method according to claim 33, wherein the volatile memory device is a synchronous static random access memory.

36. The method according to claim 35, wherein the synchronous static random access memory has a discontinuous clock through out the bootstrapping procedure.

37. A mechanism for bootstrapping a processor from a volatile memory device connected to the processor, comprising the steps of:

means for bootstrapping a master processor from flash device;

means for asserting reset lines of the processor;

means for loading boot code for the processor from the flash device into the volatile memory device; and

means for de-asserting the reset lines of the processor, wherein the processor performs the bootstrap procedure using the boot code stored in the volatile memory device.

38. The mechanism of claim 37, wherein the memory control signals of the second processor and hardware handshake signals of the volatile memory device are combined to imitate a boot from a flash device.

39. The mechanism of claim 37, wherein a complex programmable logic device generates the reset lines of the processor.

40. The mechanism of claim 37, wherein the reset lines are controlled by the master processor.

41. The mechanism of claim 38, wherein a complex programmable logic device comprises logic units to correctly combine the memory control signals of the second processor and the hardware handshake signals of the volatile memory device.

42. The mechanism of claim 37, wherein a plurality of processors are bootstrapped by loading the boot code for the plurality of processors into a plurality of volatile memory devices, wherein each processor is connected to a different volatile memory device.

43. The mechanism of claim 42, wherein the master processor provides identity to each of the plurality of processors by posting information through shared memory.

44. The mechanism of claim 37, wherein the volatile memory device is static random access memory.

45. The mechanism of claim 37, wherein the volatile memory device is dual port random access memory.

46. The mechanism of claim 44, wherein the volatile memory device is a synchronous static random access memory.

47. The mechanism of claim 45, wherein the memory control signals static random access memory has a discontinuous clock through out the bootstrapping procedure.